Claims

We claim:

1. A method of forming an integrated circuit device, comprising the steps of:

forming a pair of interconnection patterns on a substrate, the substrate having a semiconductor region disposed between the pair of interconnection patterns;

forming an etch-stop layer on the pair of interconnection patterns and the substrate; then

forming a sacrificial insulation layer comprising a first material on the pair of interconnection patterns and on the semiconductor region;

selectively etching the sacrificial insulation layer to expose portions of the etch-stop layer extending on surfaces of the pair of interconnection patterns;

forming sidewall insulation spacers that comprise a second material and extend on sidewall portions of the pair of interconnection patterns in an upper gap region between the pair of interconnection patterns and on a portion of the sacrificial insulation layer covering the semiconductor region; and

selectively etching the portion of the sacrificial insulation layer covering the semiconductor region to define recesses underneath the sidewall insulation spacers, using the sidewall insulation spacers as an etching mask.

2. A method as recited in Claim 1, further comprising the steps of:

etching a portion of the etch-stop layer that is exposed by the step of selectively etching the portion of the sacrificial insulation layer covering the semiconductor region to define recesses underneath the sidewall insulation spacers from the surface of the semiconductor region; and

forming a conductive pad between the pair of interconnection patterns such that the conductive pad engages the semiconductor region.

3. A method as recited in Claim 1, wherein the step of selectively etching the portion of the sacrificial insulation layer covering the semiconductor region to define recesses underneath the sidewall insulation spacers comprises the step of:

selectively etching the portion of the sacrificial insulation layer covering the semiconductor region to define recesses underneath the sidewall insulation spacers while maintaining the sacrificial insulation layer on sidewall portions of the pair of interconnection patterns in a lower gap region between the sidewall insulation spacers and the substrate.

4. A method as recited in Claim 1, wherein the step of selectively etching the portion of the sacrificial insulation layer covering the semiconductor region to define recesses underneath the sidewall insulation spacers comprises the step of:

selectively etching the portion of the sacrificial insulation layer covering the semiconductor region to define recesses underneath the sidewall insulation spacers such that the sacrificial insulation layer is removed from sidewall portions of the pair of interconnection patterns in a lower gap region between the sidewall insulation spacers and the substrate.

5. A method as recited in Claim 1, wherein the etch-stop layer has a thickness of approximately 200Å to approximately 1000Å.

6. A method as recited in Claim 1, wherein the etch-stop layer is comprised of the second material.

7. A method as recited in Claim 1, wherein the second material comprises silicon nitride (SiN).

8. A method as recited in Claim 1, wherein the first material comprises a material selected from the group consisting of high density plasma (HDP) oxide, plasma-enhanced tetraethyl ortho silicate (PE-TEOS), and undoped silicate glass (USG).

9. A method as recited in Claim 1, wherein the step of forming the sacrificial insulation layer is performed at a temperature less than approximately 800°C.

10. A method as recited in Claim 1, wherein the step of selectively etching the sacrificial insulation layer to expose portions of the etch-stop layer extending on surfaces of the pair of interconnection patterns comprises the step of:

isotropically etching the sacrificial insulation layer to expose portions of the etch-stop layer extending on surfaces of the pair of interconnection patterns.

11. A method as recited in Claim 1, wherein the step of selectively etching the portion of the sacrificial insulation layer covering the semiconductor region to define recesses underneath the sidewall insulation spacers comprises the step of:

anisotropically etching the portion of the sacrificial insulation layer covering the semiconductor region to define recesses underneath the sidewall insulation spacers.

12. A method of forming an integrated circuit device, comprising the steps of:

forming an isolation layer in a substrate to define a memory cell region and a peripheral circuit region;

forming a pair of word line patterns on the substrate in the memory cell region;

forming a gate pattern in the peripheral circuit region;

forming a sacrificial insulation layer between the pair of word line patterns such that a gap between the pair of word line patterns is substantially filled;

etching the sacrificial insulation layer such that the sacrificial insulation layer fills a lower gap region between the pair of word line patterns that is adjacent the substrate; and

forming an interlayer insulation layer on the memory cell region and the peripheral circuit region such that a distance from an upper surface of the interlayer insulation layer to the substrate surface in the memory cell region is greater than a distance from the upper surface of the interlayer insulation layer to the substrate in the peripheral circuit region.

13. A method as recited in Claim 12, further comprising the steps of:

etching the interlayer insulation layer from the memory cell region;

etching the sacrificial insulation layer to expose the substrate between the word line patterns; and

forming a conductive layer on the memory cell region and the peripheral circuit region such that a distance from an upper surface of the conductive layer to the substrate surface in the memory cell region is greater than a distance from the upper surface of the conductive layer to the substrate in the peripheral circuit region.

14. A method as recited in Claim 13, further comprising the step of:

etching the conductive layer in the memory cell region and the conductive layer and the interlayer insulation layer in the peripheral circuit region to form a conductive pad in the gap between the pair of word line patterns.

15. A method as recited in Claim 13, wherein the step of etching the conductive layer in the memory cell region and the conductive layer and the interlayer insulation layer in the peripheral circuit region is performed using chemical mechanical polishing (CMP).

16. A method as recited in Claim 12, further comprising the steps of:

forming a spacer insulation layer on the etched sacrificial insulation layer and the pair of word line patterns such that the spacer insulation layer is disposed on sidewalls of the pair of word line patterns in an upper gap region between the pair of word line patterns that is remote from the substrate;

etching the spacer insulation layer to expose a portion of the sacrificial insulation layer between the pair of word line patterns while maintaining the spacer insulation layer on the sidewalls of the pair of word line patterns in the upper gap region; and

etching the interlayer insulation layer and the sacrificial insulation layer to expose the substrate between the word line patterns while maintaining the sacrificial insulation layer on the sidewalls of the pair of word line patterns in the lower gap region, the lower gap region being wider than the upper gap region.

17. An integrated circuit device, comprising:

a substrate;

an interconnection pattern having sidewalls disposed on the substrate; and

a composite insulation layer that comprises a first material layer and a second material layer disposed on the sidewalls such that the first material layer is disposed in an upper sidewall region and the second material layer is disposed in a lower sidewall region between the first material layer and the substrate, the first material layer being thicker than the second material layer.

18. An integrated circuit device as recited in Claim 17, wherein the substrate comprises a semiconductor region disposed adjacent to the interconnection pattern.

19. An integrated circuit device as recited in Claim 18, further comprising:

a conductive pad that abuts against the composite insulation layer on one of the interconnection pattern sidewalls and engages the semiconductor region.

20. An integrated circuit device as recited in Claim 17, wherein the interconnection pattern comprises:

a conductive layer; and

a cap layer disposed on the conductive layer; and wherein the integrated circuit device further comprises:

a gate insulation layer interposed between the conductive layer and the substrate.

21. An integrated circuit device as recited in Claim 20, wherein the second material layer overlaps an interface between the conductive layer and the cap layer.

22. An integrated circuit device as recited in Claim 17, wherein the second material layer comprises a material selected from the group consisting of high density plasma (HDP) oxide, plasma-enhanced tetraethyl ortho silicate (PE-TEOS), and undoped silicate glass (USG).

23. An integrated circuit device as recited in Claim 17, wherein the first material layer comprises silicon nitride (SiN).